## REMARKS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 43-74, 83, 84 and 89-102 are pending. Claims 43-74, 83, 84 have been currently amended. Claims 89-102 have been newly added. Claims 1-42, 75-82 and 85-88 have been canceled. No new matter is believed to be added herein.

Response to Claim Rejections under 35 U.S.C. 102 and 103

Applicant respectfully traverses the rejections for at least the reasons set forth below.

**Response to Claims 43-63**

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As currently amended, independent Claim 43 is recited below:

43. A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said dielectric layer, wherein said passivation layer comprises silicon nitride; and

a circuit trace over said passivation layer.

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*Reconsiderations of Claims 43 and 48-55 rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al. (US 6,495,442), of Claims 44-46 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Leidy (US 2003/0155570), of Claims 45 and 47 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Simila (US 2003/0183332), and of Claims 54-63 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Carichner et al. (US 5,972,734) are requested in accordance with the following remarks.*

Applicant respectfully asserts that the chip structure claimed in Claim 43 patentably distinguishes over the citations by Lin et al. (US 6,495,442).

Lin et al. fail to teach, hint or suggest the subject matter that "a circuit trace over a passivation layer is connected to a resistor in a silicon substrate", as claimed in Claim 43.

The Examiner considers that "It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin to have the resistor made of silicon and a dopant of boron, phosphorous, or arsenic as in Leidy in order to be able to predetermine the device resistivity". *~ See lines 4-7, in the last paragraph of page 3, in the last Office Action mailed Jun. 13, 2007 ~*

Applicant respectfully traverses the Examiner's opinion because the resistor made of silicon with a dopant, as taught by Leidy, is typically used to be connected to a circuit trace under a passivation layer. Even though the resistor made of silicon with a dopant, as taught by Leidy, could be added to the Lin et al.'s device, it is believed that the resistor made of silicon with a dopant, as taught by Leidy, should not be connected to a circuit

trace over a passivation layer, but should be connected to a circuit trace under a passivation layer, as taught by Leidy.

Withdrawal of rejection under 35 U.S.C.102(b) to Claim 43 is respectfully requested.

For at least the foregoing reasons, applicant respectfully submits independent Claim 43 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 44-63 patently define over the prior art as well.

**Response to Claims 64-74, 83 and 84**

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As currently amended, independent Claim 64 is recited below:

64. A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said dielectric layer; and

a circuit trace over said passivation layer, wherein said circuit trace is connected to said resistor, and wherein said circuit trace comprises a

titanium-containing layer and a gold layer over said titanium-containing layer.

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*Reconsiderations of Claims 64 and 69-76 rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al. (US 6,495,442), of Claims 65-67 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Leidy (US 2003/0155570), of Claims 66 and 68 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Simila (US 2003/0183332), and of Claims 75-84 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Carichner et al. (US 5,972,734) are requested in accordance with the following remarks.*

Applicant respectfully asserts that the chip structure claimed in Claim 64 patentably distinguishes over the citations by Lin et al. (US 6,495,442).

Lin et al. fail to teach, hint or suggest the subject matter that "a circuit trace over a passivation layer is connected to a resistor in a silicon substrate", as claimed in Claim 64.

The Examiner considers that "It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin to have the resistor made of silicon and a dopant of boron, phosphorous, or arsenic as in Leidy in order to be able to predetermine the device resistivity". *~ See lines 4-7, in the last paragraph of page 3, in the last Office Action mailed Jun. 13, 2007 ~*

Applicant respectfully traverses the Examiner's opinion because the resistor made of silicon with a dopant, as taught by Leidy, is typically used to be connected to a circuit trace under a passivation layer. Even though the resistor made of silicon with a dopant, as taught by Leidy, could be added to the Lin et al.'s device, it is believed that the resistor made of silicon with a dopant, as taught by Leidy, should not be connected to a circuit

trace over a passivation layer, but should be connected to a circuit trace under a passivation layer, as taught by Leidy.

Withdrawal of rejection under 35 U.S.C.102(b) to Claim 64 is respectfully requested.

For at least the foregoing reasons, applicant respectfully submits independent Claim 64 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 65-74, 83 and 84 patently define over the prior art as well.

Conclusion

Some or all Claims are believed to be in condition for Allowance, and that is so requested.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)